Charge-domain signal clamping and extended dark signal cancellation for automotive CMOS image sensors

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Abstract — This paper presents circuit techniques to enhance the image quality of CMOS image sensors for automotive applications under harsh conditions such as high illumination and high temperature. A charge-domain clamping at the unit pixel level is proposed to constrain the voltage swing within the ADC full-scale range, and improve linearity of pixel source follower. To maintain black level stability at high temperatures, an extended dark signal cancellation scheme is introduced, to increase temperature coverage without sacrificing A/D conversion time. From the measurement results, the proposed charge-domain clamping improves the linearity of pixel output by 27.8% compared to conventional methods, and the extended dark signal cancellation ensures stable black level at a temperature up to Tj 120°C at 11-ms exposure time in a given A/D conversion time.

I. INTRODUCTION

In the advanced driver assistance systems (ADAS) and autonomous driving (AD) applications, a CMOS image sensor (CIS) plays an important role in object detection for vehicle safety. The automotive image sensor should stream out video with no saturation and no degradation on the black level (or, pedestal level), regardless of the illuminance conditions and temperatures, to achieve a high dynamic range (HDR) [1]. One of the approaches to achieve HDR is to read out pixel signals in multiple times with different conversion gains in a single exposure, using a split-PD structure [2]–[4]. Fig. 1(a) shows a block diagram of a typical CIS with column-parallel ADC architecture for high ADC throughput supporting multiple readouts per pixel, and split-PD pixel structure is shown in Fig. 1(b). In this structure, the high conversion gain (HCG) readout has the lowest reference voltage among other readouts due to strong coupling from the reset gate (RG) and the dual conversion reset gate (DRG). This low reference level restricts the applicable pixel output range in HCG readout. Furthermore, at a strong light condition, HCG readout is vulnerable for band noise, which is a horizontal band adjacent to a light source [5].

Automotive CMOS image sensors usually operate at high temperatures, because they are typically mounted on the vehicle's exterior or behind the windshield; they are frequently exposed to high temperatures. There are several problems caused by the high temperature. One of the major challenges is the dark signal, which increases with temperature [6], [7]. In a conventional dark signal

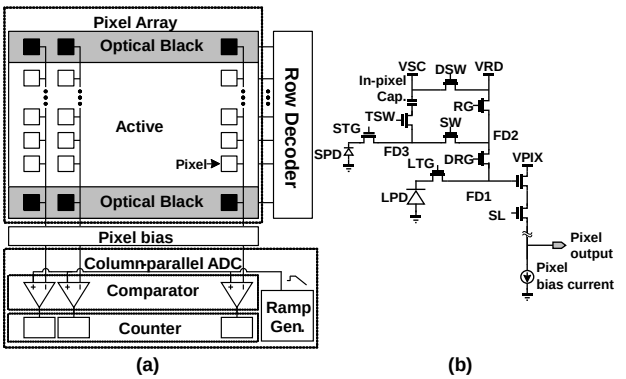

Fig. 1: A diagram of the image sensor structure and its pixel: (a) block diagram of image sensor with column-parallel single-slope ADC, (b) unit pixel schematic with two photo diodes for automotive image sensors.

cancellation, the dark level of the optical black (OB) pixels is subtracted from the active pixel signal, in a digital domain with a fixed bit resolution. Hence, the coverage of the conventional approach will be limited by an ADC bit resolution; at high temperatures, failure in dark signal cancellation may cause color distortion due to black level imbalance. To avoid it, we may increase the dark signal coverage by performing A/D conversion with higher bit resolution. However, it is not practical as it increases the A/D conversion time, which limits the frame rate.

In this paper, we propose two approaches for improved immunity to high illumination and high temperature: charge-domain clamping and dark signal cancellation extension. Charge-domain clamping improves pixel output linearity and also suppresses band noise, as in the conventional method. Dark signal cancellation coverage can be extended by cancelling dark signal partially at the analog domain.

II. BACKGROUND

A. Pixel signal clamping

Under strong light conditions, the voltage output of a pixel may drop significantly, which leads to incorrect signal readout. To avoid this issue, the pixel output should be limited by a dedicated clamp circuit. One of the conventional clamp circuits operates at a voltage domain, which consists of a source follower and a voltage source (VCLP1), as shown in Fig. 2(a). It is connected to the pixel output by sharing the same bias current source.

The pixel output drops in proportion to the intensity of

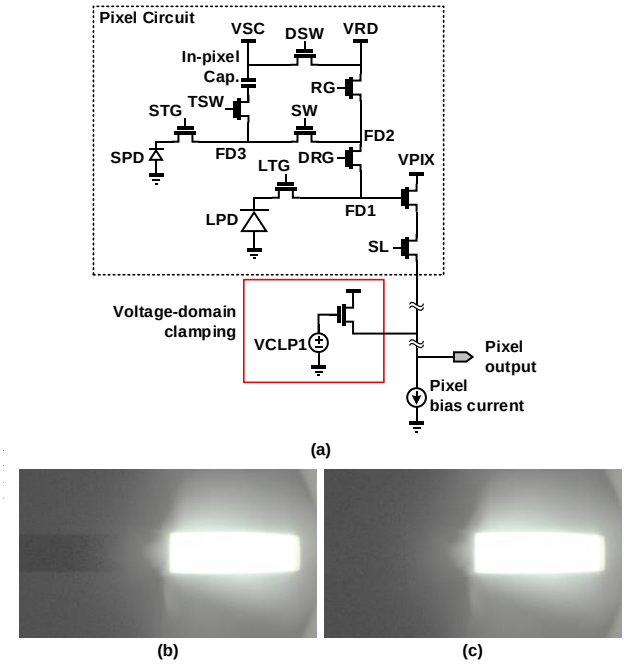

Fig. 2. (a) Conventional voltage-domain clamping scheme with pixel schematic, which uses a dedicated circuit. (b) Image of band noise without clamping. (c) Image of band noise suppressed by clamping.

light and integration time. The source follower in the pixel initially supplies the pixel bias current, whereas the source follower in the voltage-domain clamp circuit is turned off, because VCLP1 is usually set below the reset voltage of the pixel at FD1. When the pixel output voltage drops further to turn on the clamp circuit, the clamp circuit begins to share the pixel bias current. Eventually, when the clamp circuit takes over the entire pixel bias current, pixel output does not further decrease to stay at a fixed voltage level. Thus, the minimum voltage of a pixel output can be controlled by VCLP1, which should be set carefully. Due to the finite transconductance of the clamp circuit, the linearity of the pixel output is disrupted near the current-sharing region. Hence, the upper limit of VCLP1 should be set to ADC full-scale range plus the voltage margin to secure linearity. On the other hand, lower limit of the VCLP1 is determined by ensuring operation mode of the pixel bias current source at saturation region. All in all, the design space for VCLP1 will be very limited considering both upper and lower limits. If the pixel output voltage drops significantly low at high illumination, the pixel bias current will go into triode region to reduce bias current. In this case, power fluctuation will occur to affect the whole activated columns in column-parallel readout, which leads to band noise [5]. Fig2. (b) shows band noise, while Fig2. (c) demonstrates its suppression by the clamping technique.

B. Dark signal cancellation

Image sensors are expected to output images which is linearly proportional to light intensity. However, dark signal, which is generated by the dark current in the photodiode and increases with the temperature, will be added as an offset signal to deteriorate image quality. Conventional approach to cancel dark signal cancellation is to read out the dark signal from the OB pixels, and to

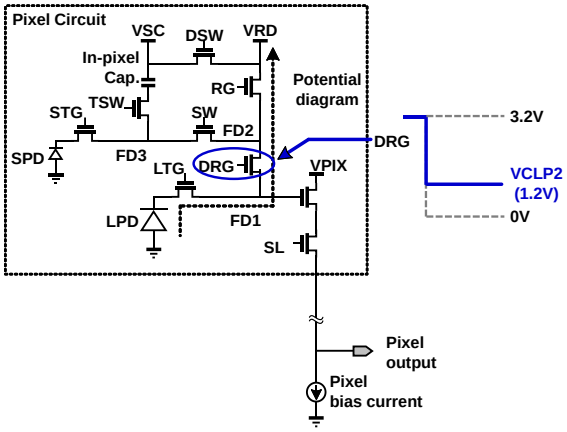

Fig. 3. Proposed charge-domain clamping scheme. This scheme utilizes the DRG transistor in a pixel.

subtract it from the active pixel signal in the digital domain. The image output (I_{conv}) from a conventional dark signal cancellation is expressed by (1), as follows:

$$I_{conv} = S_{act} + S_{dark,act} - \min\left[S_{dark,OB},\ S_{clip}\right] \qquad (1)$$

where, S_{act}, $S_{dark,act}$ denote the light-dependent signal and dark signal from active pixel, respectively, whereas $S_{dark,OB}$ and S_{clip} are dark signal from OB pixel and clipping value, respectively. Ideally, $S_{dark,OB}$ should be equal to $S_{dark,act}$ for successful dark signal cancellation. However, if $S_{dark,OB}$ is significantly large, full saturation code of I_{conv} cannot be guaranteed. Thus, S_{clip} is used to limit the maximum coverage of the dark signal cancellation. For example, in the case of a 12.5-bit analog-to-digital converter for a 12-bit image, the clipping value should be set lower than 1700, to represent the full 12-bit code (4096). At a high junction temperature (Tj) of > 105°C, a large $S_{dark,OB}$, far exceeding the S_{clip} value, will be generated, raising the black level even in the absence of incident light. This leads to color distortion in images, which corrupts image quality and system performance. This issue would be mitigated by increasing S_{clip}. However, it requires additional A/D conversion time, which limits maximum frame rate.

III. Proposed Schemes

A. Pixel signal clamping at charge-domain

Fig. 3 shows the concept of the proposed charge-domain clamping, which controls the turn-off voltage of the DRG signal by the clamp voltage of VCLP2. Fig. 4(a) presents a timing diagram for the HCG readout. For a higher conversion gain, the capacitance of the FD1 can be decreased by turning off RG and DRG. With the HCG readout, the pixel can produce a large voltage swing in a given number of electrons. However, turning off both RG and DRG leads to large capacitive coupling to lower reset levels of HCG readout. Therefore, the voltage margin of the pixel bias current source is degraded due to a significant voltage drop under high illumination, as discussed in the previous section. This issue can be addressed by the proposed clamping scheme. Fig. 4(b) illustrates a potential diagram of a pixel with the charge-domain clamping. The potential barrier of DRG is

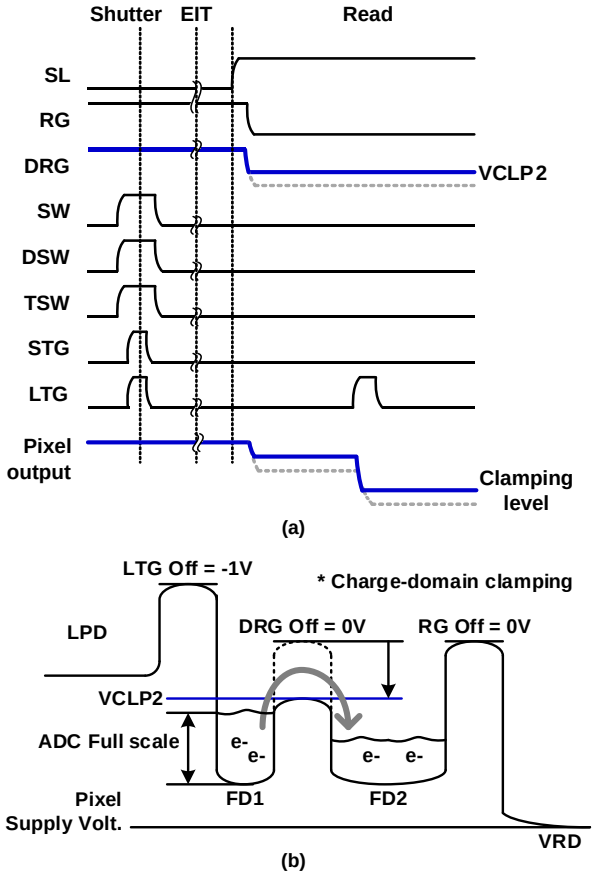

Fig. 4. (a) Timing diagram for the pixel control signals and pixel output for charge-domain clamping. (b) Potential diagram including LPD, FD1, FD2, DRG and RG with charge-domain clamping operation enabled and disabled

controlled by the VCLP2 level. When VCLP2 is turned off slightly (say, 1.2 V), the potential barrier of the DRG becomes lower to move the electrons at FD1 partially into FD2. Hence, the VCLP2 level limits excessive charge accumulation above the ADC full-scale range at FD1.

The charge-domain clamping ensures that the pixel bias current source remains in the saturation region. As shown in Fig. 5, the proposed clamping scheme can extend the linear output region of the pixel compared to that of voltage-domain clamping. As the swing level of the DRG signal is reduced by VCLP2, the amount of capacitive coupling at FD1 decreases. Therefore, the reset level increases by 175 mV (from 1.87 V to 2.04 V) with the proposed scheme in our 3-µm pixel circuit, as shown in Fig. 5. Thus, the linear output range is increased from 734mV to 939mV with a 27.8% improvement over the conventional method, while still suppressing band noise.

B. Dark signal cancellation at mixed-signal domain

In order to increase dark signal cancellation coverage, we propose a mixed-signal domain approach to subtract the dark signal partially in the analog domain before dark signal cancellation in the digital domain. Fig. 6(a) presents a conceptual block diagram of the proposed dark signal cancellation scheme. Once the dark signal from the OB pixels is measured, the "partial" dark offset, which will be compensated in the analog domain during A/D conversion, is computed by the analog offset controller; this partial

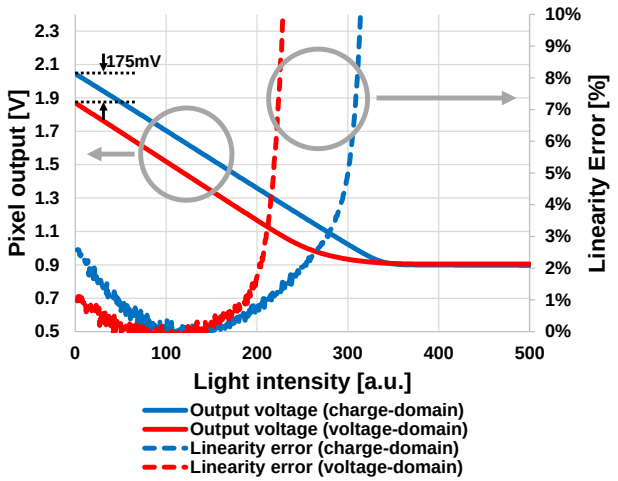

Fig. 5. Results of the clamping methods by simulation. Comparison of linearity between voltage-domain clamping and charge-domain clamping.

dark offset relieves the amount of dark signal to be compensated at the digital domain within an acceptable range. The partial dark offset is then applied to the ramp generator, which adjusts the negative offset of the ramp signal. Finally, the same amount of partial dark offset that was applied to the ramp signal is added in the digital domain. This process is expressed in (2) for the image output of the proposed dark signal cancellation (I_{prop}):

$$I_{prop} = S_{act} + S_{dark,act} - S_{ramp\_os} - \min\left[S_{dark,OB},\ S_{clip}\right] + S_{dark\_os} \quad (2)$$

where S_{ramp_os} and S_{dark_os} denote the partial dark offset applied to the ramp generator and the same amount of partial dark offset for digital-domain compensation, respectively. Thanks to the proposed scheme, a higher S_{clip} value can be used to effectively extend dark signal cancellation coverage by S_{dark_os} in a given A/D conversion time, ensuring the black level in the output image stable at Tj 105°C or higher.

Fig. 6(b) shows the ramp waveforms and A/D conversion periods for the conventional and proposed methods for the same dark signal cancellation coverage. The proposed dark signal cancellation requires a shorter A/D conversion time, compared to the conventional one. To increase dark signal cancellation coverage by 1024 codes, the proposed method can save A/D conversion time by 15% compared to the conventional approach.

Fig. 7(a) shows the measurement results for temperature dependency in the black level with and without the extended dark signal cancellation, where all measurements were performed with the same A/D conversion time and exposure time of 11 ms. Without the extended dark level cancellation (red), the output code increases from Tj 105°C. But, applying the proposed method (blue), the output code remains at a constant value up to Tj 120°C, with a 14% extension in the operating temperature range compared to the conventional method. By the aid of the proposed scheme, the captured image is not degraded at Tj 120°C, as observed in the captured images in Fig. 7(b).

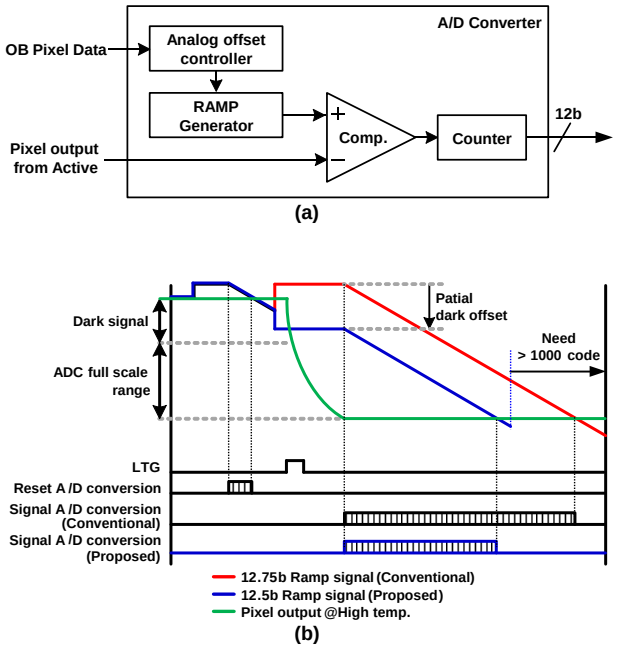

Fig. 6. (a) Block diagram of the extended dark signal cancellation scheme and (b) representation of ramp signal with ADC operations for the conventional and extended dark signal cancellation.

IV. Conclusion

This paper demonstrated that charge-domain clamping and extended dark signal cancellation techniques improve image quality in extreme lighting and high-temperature conditions. The charge-domain clamping increases linearity of pixel output by 27.8%, and the extended dark signal cancellation enhances operating temperature range by 14% in a given A/D conversion time. Therefore, the proposed ideas help to extend high dynamic range effectively without sacrificing frame rate, making it suitable for automotive CMOS image sensors. These schemes are implemented on a 5-Mpixel 130-dB single-exposure HDR automotive image sensor with 3-µm split-PD pixel, operating at 60 fps. The chip micrograph is shown in Fig. 8, which is fabricated in a two-stack process with top die for pixel and bottom die for analog and digital circuitry.

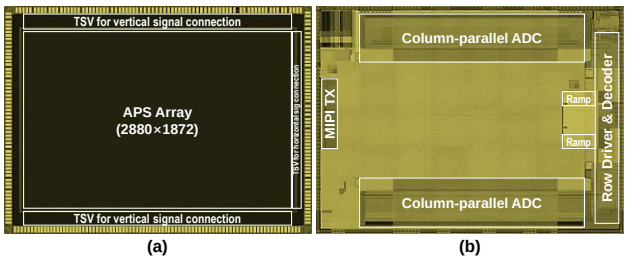

Fig. 8. IC micrograph of the proposed automotive image sensor (a) top die for pixel array and (b) bottom die for logic

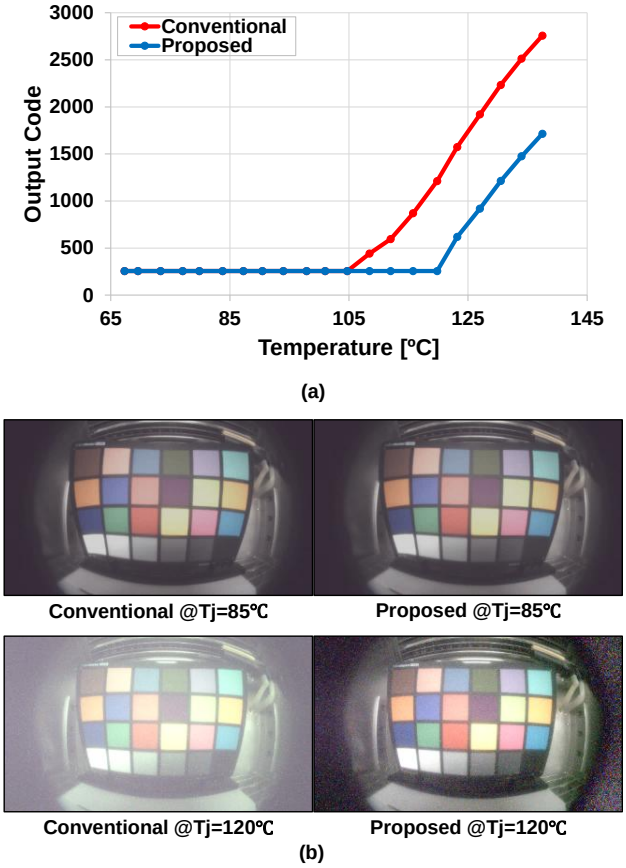

Fig. 7. Performance comparison between conventional and proposed dark signal cancellation methods: (a) measurement results of black level with temperature, and (b) captured images at Tj 85°C and 120°C.

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